What is claimed is:

1. A ferroelectric capacitor comprising:

a bottom electrode which has a plate portion and a projecting portion, wherein the projecting portion is arranged on a central area of the plate portion;

a dielectric layer formed on a peripheral area of the bottom electrode;

a ferroelectric layer formed on the dielectric layer and on the projection portion of the bottom electrode; and

a top electrode formed on the ferroelectric layer.

2. The ferroelectric capacitor of claim 1, wherein the ferroelectric layer includes a damaged area which is formed on the dielectric layer.

3. The ferroelectric capacitor of claim 1, wherein the bottom electrode comprises the plate portion and the projecting portion as single unitary electrode.

4. The ferroelectric capacitor of claim 1, wherein a top surface of the dielectric layer is substantially coplanar with aligned a top surface of the projecting portion.

5. The ferroelectric capacitor of claim 1, wherein a side surface of the plate portion of the bottom electrode, a side surface of the dielectric layer, a side surface of the ferroelectric layer and a side surface of the top electrode are aligned.

6. The ferroelectric capacitor of claim 1, wherein the bottom electrode and the top electrode are made of an oxidation resistance metal or a conductive metal oxide.

7. The ferroelectric capacitor of claim 1, wherein the plate portion of the bottom electrode and the projection portion of the bottom electrode are made of different material.

8. The ferroelectric capacitor of claim 7, wherein the plate portion of the bottom electrode includes a lower layer and an upper layer.

9. The ferroelectric capacitor of claim 8, wherein the projection portion of the bottom electrode is made of platinum.

10. A ferroelectric capacitor comprising:

a bottom electrode;

a top electrode;

a ferroelectric layer formed between the bottom electrode and the top electrode; and

a dielectric spacer formed between the bottom electrode and the top electrode, wherein the dielectric spacer decreases an electric field strength at a peripheral area of the capacitor.

11. The ferroelectric capacitor of claim 10, wherein the bottom electrode includes a projecting portion arranged at a central area of the bottom electrode, and wherein the dielectric spacer is arranged around the projecting portion.

12. The ferroelectric capacitor of claim 10, wherein a distance between the bottom electrode and the top electrode at a peripheral area of the capacitor is grater than a distance between the bottom electrode and the top electrode at a central area of the capacitor.

13. The ferroelectric capacitor of claim 10, wherein a side surface of the bottom electrode, a side surface of the ferroelectric layer, a side surface of the dielectric spacer and a side surface of the top electrode are aligned.

14. A ferroelectric capacitor comprising:

a first electrode which has a plate portion and a projecting portion, wherein the projecting portion is arranged on a central area of the plate portion;

a spacer layer formed on a peripheral area of the first electrode;

a ferroelectric layer formed on the dielectric spacer and on the projecting portion; and

a second electrode formed on the ferroelectric layer.

15. The ferroelectric capacitor of claim 14, wherein a side surface of the plate portion of the first electrode, a side surface of the ferroelectric layer and a side surface of the

second electrode are aligned.

16. A semiconductor device comprising:

a semiconductor substrate;

a switching transistor formed on the semiconductor substrate, the switching transistor having a source region, a drain region and a gate electrode;

an insulating layer formed on the semiconductor substrate and the switching transistor;

a ferroelectric capacitor formed on a top surface of the insulating layer, the ferroelectric capacitor including

a bottom electrode formed on the insulating layer, the bottom electrode having a plate portion and a projecting portion, wherein the projecting portion is arranged on a central area of the plate portion,

a dielectric layer formed on the peripheral area of the bottom electrode,

a ferroelectric layer formed on the dielectric layer and on the protecting portion, and

a top electrode formed on the ferroelectric layer; and

a plug electrode which is embedded in the insulating layer, wherein the plug electrode connects the source region of the switching transistor to the bottom electrode of the ferroelectric capacitor.

17. The semiconductor device of claim 16, wherein the top surface of the insulating layer is formed substantially flat.

18. The semiconductor device of claim 16, wherein the ferroelectric capacitor is located over the source region of the switching transistor.

19. A semiconductor device comprising:

a semiconductor substrate;

a switching transistor formed on the semiconductor substrate, the switching transistor having a source region, a drain region and a gate electrode;

an insulating layer formed on the semiconductor substrate and the switching transistor;

a ferroelectric capacitor formed on a top surface of the insulating layer, the ferroelectric capacitor including

a bottom electrode formed on the insulating layer, the bottom electrode has a plate portion and a projecting portion, wherein the projecting portion is arranged on the central area of the plate portion,

a dielectric layer formed on a peripheral area of the bottom electrode,

a ferroelectric layer formed on the dielectric layer and on the projecting portion, and

a top electrode formed on the ferroelectric layer; and

a wiring which connects the source region of the switching transistor to the top electrode of the ferroelectric capacitor.

20. The semiconductor device of claim 19, wherein the wiring includes a plug

portion which extends from the source region of the switching transistor to the top surface of the insulating layer and a wiring portion which connects a top of the plug to the top electrode of the ferroelectric capacitor.